

Model Name: AXM22001-2A-C

Key Features

- Integrated 2.4GHz, IEEE 802.11b/g compatible WiFi connectivity
- Integrated PCB antenna
- Max outdoor range up to 300m (984 ft.), line of sight
- Supports operation in Infrastructure or Ad-Hoc (IBSS) network topology
- Supports 802.11i security: WEP-64/128, TKIP (WPA-PSK) and AES (WPA2-PSK)
- Dual 8-bit 1T 8051/80390 CPU @ 80MHz
- 1MB shared Flash memory for MCPU and WCPU program code and configuration data storage
- 64KB data memory for MCPU
- 4 UART interfaces
- High Speed SPI interface (master or slave mode)
- I2S or PCM interface
- Local Bus host interface (master or slave mode)
- MII or RMII interface
- I2C interface
- Up to 32 GPIOs (4 GPIO ports of 8 bits each)
- Supports real-time clock, with option to use independent power supply from lithium battery
- Supports TCP, UDP, ICMP, IGMP, IPv4, DHCP, BOOTP, ARP, DNS, SMTP, SNTP, UPnP, PPPoE and HTTP in software
- Supports network boot over Ethernet or WiFi using BOOTP and TFTP
- Single operating voltage: 3.3V typical
- Board size: 51.0mm x 28.0mm x 4.5mm surface mountable module

Applications

- Serial to WiFi Device Server
- WiFi Speaker
- WiFi Remote Control/Monitor
- Ethernet to WiFi Bridge
- Zigbee to WiFi Bridge
- WiFi Network Camera
- WiFi RFID
- SPI to WiFi Bridge
- TCP/IP and WLAN Offload Co-processor
- WiFi Internet Radio

Document No: AXM22001-2A-C/V1.01/11/07/11



The AXM22001-2A-C is a 2.4GHz 802.11b/g WiFi module board which integrates AX22001 and Airoha AL2230S RF transceiver on board to provide a complete WiFi module solution with various user or host interfaces supported. The AXM22001-2A-C is a surface mountable module with castellated mounting holes which offers smaller-form-factor, lower-cost, pre-calibrated RF front-end and pre-certified WiFi module board to free the user from RF and antenna design tasks and regulatory compliance testing, ultimately providing quicker time to market. The user can design his host board with desired function and interface circuits and assemble it with the AXM22001-2A-C WiFi module board through the castellated mounting holes.

1



Pinout Diagram of Castellated Mounting Holes



Figure 1. Module pinout



Pin Description of Castellated Mounting Holes

Pin type abbreviation:

PI: Power input B: Bidirectional signal pin PO: Power output I: Input signal pin

G: Ground O: Output signal pin

Pin No Symool run No Pin No Symool run No 1 13.1 3V3_PAS PI 3.3V power input for RF power amplifier 2 J3.2 3V3_PAS PI 3.3V power input for RF power amplifier 3 J3.3 GND G Ground 4 13.4 GND G Ground 5 J3.5 GND G Ground 6 J2.1 GND G Ground 7 J2.2 GND G Ground 8 J2.3 P20* B P21/LA5/RXD1/MDC signals 9 J2.4 P21* B P21/LA7/WRXD0 signals 10 J2.6 P23* B P23/LAE/RCIK /VXD0 rymole CK signals 11 J2.6 P23* B P23/LLAS/N/XD2/TML_CK signals 12 J2.7 P24* B P24/LDS/N/XD2/TML_CK signals 13 J2.8 P25* B P23/LLDS/N/TXD2/TML_CK signals 14 J2.9 XT132KI	Module	Schematic	Pin Name	Pin	Description		
1 3.1 3V3 PAS PI 3.5V power input for RF power amplifier 3 J3.3 GND G Ground Ground 4 J3.4 GND G Ground Ground 5 J3.5 GND G Ground Ground 6 J2.1 GND G Ground Ground 7 J2.2 GND G Ground Ground 8 J2.3 P20* B P20/LA5/RXD0 signals 10 J2.5 P22* B P22/LA7/RXD0 signals 11 J2.6 P23* B P23/LALE/PCLK / WTXD0 signals 12 J2.7 P24* B P25/LINT / XND / TM0 GT signals 13 J2.8 P25* B P25/LINT / XND / TM1 GT signals 14 J2.9 P26* B P26/LDS N/RXD2 / TM1 GT signals 15 J2.10 P27* B P27/LUDS N/RXD2 / TM1 GT signals 14 J2.9 P26* B P26/L	PIN NO	Symbol Pin No	21/2 DAG	Type			
2 3.4 3.4 SV pNS P1 3.5.V power input for KP power amplifier 3 J3.3 GND G Ground 4 J3.4 GND G Ground 5 J3.5 GND G Ground 6 J2.1 GND G Ground 7 J2.2 GND G Ground 8 J2.3 P20* B P21/LA6/TXD1/MDIC signals 9 J2.4 P21* B P21/LA6/TXD1/MDIC signals 10 J2.5 P22* B P22/LA7/WRXD0 signals 11 J2.6 P23* B P24/LRDY/DVP_RDY/RXD3/TM0_CK signals 12 J2.7 P24* B P24/LRDY/DVP_RDY/RXD3/TM0_CK signals 14 J2.9 P26* B P26/LDS N/TXD2/TM1_CK signals 14 J2.9 P26* B P26/LDS N/TXD2/TM1_CK signals 15 J2.10 P27*L32KG O 32.768KHz crystal input 17 J2.12	1	J3.1	3V3_PAS	PI	3.3V power input for RF power amplifier		
3 J.3. GND G Ground 4 J3.4 GND G Ground 5 J3.5 GND G Ground 6 J2.1 GND G Ground 7 J2.2 GND G Ground 8 J2.3 P20* B P20 / LA5 / RXD1 / MDC signals 10 J2.5 P22* B P22 / LA7 / WRXD0 signals 11 J2.6 P23* B P23 / LALE / PCLK / WTXD0 signals 12 J2.7 P24* B P24 / LRY / DVP_RDY / RXD3 / TM0 CK signals 13 J2.8 P25* B P27 / LUDS // XTD2 / TM1 [CK signals 14 J2.9 P26* B P26 / LLDS // XTD2 / TM1 [CK signals 15 J2.10 P27* B P27 / LUDS // XTD2 / TM1 [CK signals 15 J2.10 P27* B P27 / LUDS // XTD2 / TM1 [CK signals 16 J2.11 XT132K1 J32.768KHz crystal output J1 17 <	2	J3.2	3V3_PAS	PI	3.3 v power input for RF power amplifier		
4 J.5.4 OND G Ground 5 J3.5 GND G Ground 6 J2.1 GND G Ground 7 J2.2 GND G Ground 8 J2.3 P20* B P20 / LA5 / RXD1 / MDC signals 9 J2.4 P21* B P21 / LA6 / TXD1 / MDC signals 10 J2.5 P22* B P22 / LA7 / WRXD0 signals 11 J2.6 P23* B P24 / LRDY / DVP, RDY / RXD3 / TMO_CK signals 12 J2.7 P24* B P24 / LRDY / DVP, RDY / RXD3 / TMO_CK signals 13 J2.8 P25* B P25 / LINT / TXD3 / TMO_GG rignals 14 J2.9 P26* B P26 / LLDS N / RXD2 / TMI_GT signals 15 J2.10 PZ7* B P27 / LUDS N / TXD2 / TMI_GT signals 16 J2.11 XTL32KI 1 32.768KHz crystal ottput 17 J2.12 XTL32KI 1 S2.768KHz crystal ottput	3	J3.3	GND	G	Ground		
5 J.5. GND G Ground 6 J2.1 GND G Ground 7 J2.2 GND G Ground 8 J2.3 P20* B P20/LAS/RXD1/MDC signals 10 J2.4 P21* B P21/LAS/RXD1/MDC signals 10 J2.5 P22* B P22/LA7/WRXD0 signals 11 J2.6 P23* B P23/LAE/PCLK/WTXD0 signals 12 J2.7 P24* B P23/LDS/VRXD2/TM1_CK signals 13 J2.8 P25* B P25/LUDS_N/RXD2/TM1_CK signals 14 J2.9 P26* B P26/LLDS_N/RXD2/TM1_CG signals 15 J2.10 P27* B P27/LUDS_N/TXD2/TM1_CG signals 16 J2.11 XT132KI I 32.768KHz crystal input 17 J2.14 IV8 PO 1.8V power input for 32.768KHz crystal //O and RTC logic 19 J2.14 IV8 PO 1.8V power output 12	4	J3.4	GND	G	Ground		
6 J2.1 GND G Ground 7 J2.2 GND G Ground 8 J2.3 P20* B P20/LA5/RXD1/MDC signals 9 J2.4 P21* B P21/LA6/TXD1/MDC signals 10 J2.5 P22* B P22/LA7/WRXD0 signals 11 J2.6 P23* B P23/LAE/PCLK/WTXD0 signals 12 J2.7 P24* B P24/LRDY/DVP_RDY/RXD3/TM0_CK signals 13 J2.8 P25* B P25/LINT/TXD3/TM0_GT signals 14 J2.9 P26* B P26/LIDS_N/RXD2/TM1_GT signals 16 J2.10 P27* B P26/LIDS_N/RXD2/TM1_GT signals 16 J2.13 VCC18A_RTCI P1 1.8V power output 17 J2.12 XTL32KI 1 32.768KHz crystal input 18 J2.13 VCC18A_RTCI P1 1.8V power output coutput 20 J2.14 IV& B O WiFi link status LED configurat	5	J3.5	GND	G	Ground		
7 12.2 GND G Ground 8 12.3 $P20^\circ$ B $P20 / LA5 / RXD1 / MDC signals 9 12.4 P21^\circ B P22 / LA5 / RXD1 / MDC signals 10 12.5 P22^\circ B P22 / LA7 / WRXD0 signals 11 12.6 P23^\circ B P22 / LR7 / WRXD0 signals 12 12.7 P24^\circ B P24 / LRDY / DVP_RDY / RXD3 / TM0_CT signals 13 12.8 P25^\circ B P26 / LLDS_N / RXD2 / TM1_CK signals 14 12.9 P26^\circ B P26 / LLDS_N / RXD2 / TM1_CK signals 15 J2.10 P27^\circ B P27 / LUDS_N / TXD2 / TM1_CGT signals 15 J2.10 P27^\circ B P27 / LUDS_N / TXD2 / TM1_CGT signals 16 J2.11 XTL32K1 132.768KHz crystal loput D12 17 J2.12 XTL32K1 132.768KHz crystal loput D2 10 J2.15 LB_CLK_B Local bus clock input or output D2 12 J2.16 WLD^\circ WLD^\circ $	6	J2.1	GND	G	Ground		
8 12.3 P20* B P20 / LAS / KAD / MDC signals 9 12.4 P21* P21 / LAG / TXD / MDIO signals 10 12.5 P22* B P21 / LAG / TXD / MDIO signals 11 12.6 P23* B P22 / LAT / WRXD0 signals 12 12.7 P24* B P24 / LRDY / DVP, RDY / RXD3 / TM0_CK signals 13 12.8 P25* B P25 / LINT / TXD3 / TM0_CK signals 14 12.9 P26* B P26 / LLDS N / RXD2 / TM1_CK signals 15 12.10 P27* B P27 / LUDS N / TXD2 / TM1_CK signals 16 12.11 XTL32KO 0 32.768KHz crystal input 18 12.13 VCC18A_RTCI PI 1.8V power output 18 12.13 VCC18A_RTCI PI 1.8V power output 20 12.14 1V8 PO 1.8V power output 21 12.16 WLD* O WiFi link status LED 22 1.7 SYSCK SEL I Operating sys	/	J2.2	GND	G			
9 12.4 P21* B P21/LA6 / 1ADI / MDIO signals 10 12.5 P22* P23* B P23 / LALE / PCLK / WTXD0 signals 11 12.6 P23* B P23 / LALE / PCLK / WTXD0 signals 12 12.7 P24* B P24 / LRDY / DVP, RDY / RXD3 / TM0_CK signals 13 12.8 P25* B P25 / LIDS_N / RXD2 / TM1_CK signals 14 12.9 P26* B P26 / LLDS_N / RXD2 / TM1_CK signals 16 12.11 XTL32KO O 32.768KHz crystal output 17 12.12 XTL32KI I 32.768KHz crystal output 18 D2.14 1V8 PO 1.8V power output 20 12.15 LB_CLK B Local bus clock input or output 21 12.16 WLED* O WiFi link status LED 22 12.17 SYSCK_SEL I Operating system clock frequency selection input 23 12.18 XDATA1 B XDATA1 / LB_MOD configuration 24	8	J2.3	P20*	B	P20 / LAS / RXDI / MDC signals		
10 J.2.5 P22* B P22/LA//WKD0 signals 11 J2.6 P23* B P23/LALE /PCLK /WTXD0 signals 12 J2.7 P24* B P24/LRDY /DVP_RDY /RXD3 /TM0_CK signals 13 J2.8 P25* B P25/LIDS // KXD2 /TM1_CK signals 14 J2.9 P26* B P26/LDS // KXD2 /TM1_CK signals 15 J2.10 P27* B P27/LUDS // TXD2 /TM1_GT signals 16 J2.11 XTL32K0 O 32.768KHz crystal output 17 J2.12 XTL32KI I 32.768KHz crystal output 18 J2.13 VCC18A_RTCI PI 1.8V power output 20 J2.15 LB_CLK B Local bus clock input or output 21 J2.16 WEDE*0 0 WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1/LB_MOD configuration 24 J2.90 XDATA5	9	J2.4	P21*	B	P21 / LA6 / TXDT / MDIO signals		
11 J.2.6 P23* B P23* LALE / PCLK / WIXD0 signals 12 J2.7 P24* B P25 / LINT / TXD3 / TM0_CK signals 13 J2.8 P25* B P26/LIDS_N / RXD3 / TM0_CK signals 14 J2.9 P26* B P26 / LLDS_N / RXD2 / TM1_CK signals 15 J2.10 P27* B P27/LUDS_N / TXD2 / TM1_GT signals 16 J2.11 XTL32K0 O 32.768KHz crystal output 17 J2.12 XTL32K1 I 32.768KHz crystal output 18 D2.13 VCC18A_RTC1 PI 1.8V power output 20 J2.14 IV8 PO 1.8V power output 21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1 / LB_MOD configuration 24 J2.19 XDATA2 B XDATA5 / BUNN_FLASH_EN configuration 25 J2.20 X	10	J2.5	P22*	B	P22 / LA / / WRXD0 signals		
12 12.7 $P24^*$ B $P24^*/LRDY/DYP_RDY/RUSY/TM0_CT signals 13 32.8 P25^* B P25/LLDS_N/RXDS/TM0_CT signals 14 J2.9 P26^* B P26/LLDS_N/RXDS/TM0_CT signals 15 J2.10 P27^* B P27/LUDS_N/TXD2/TM1_CT signals 16 J2.11 XTL32K0 O 32.768KHz crystal input 17 J2.12 XTL32K1 I 32.768KHz crystal input 18 J2.13 VCC18A_RTCI PI 1.8V power input for 32.768KHz crystal I/O and RTC logic 10 J2.14 IV8 PO 1.8V power output 00 21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA2 B XDATA2/SYNC_BUS configuration 24 J2.19 XDATA4 B XDATA6/IZC_BOOT_DIS configuration 25 J2.20 XDATA5 B XDATA6/IZC_BOOT_DIS configuration 27 J2.24 GND$	11	J2.6	P23*	B	P23 / LALE / PCLK / WIXDU signals		
14 J2.8 P25* B P25 / LINL / TAD5 / IMQ of signals 14 J2.9 P26* B P27 / LUDS N / TXD2 / TMI _CK signals 15 J2.10 P27* B P27 / LUDS N / TXD2 / TMI _CK signals 16 J2.11 XTL32K0 O 32.768KHz crystal output 17 J2.12 XTL32K1 I 32.768KHz crystal output 18 J2.13 VCC18A_RTCI PI 1.8V power input for 32.768KHz crystal I/O and RTC logic 20 J2.15 LB_CLK B Local bus clock input or output 21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1/LB_MOD configuration 24 J2.19 XDATA2 B XDATA5 / BURN_FLASH_921K configuration 25 J2.20 XDATA6 B XDATA6 / J2C_BOOT_DIS configuration 27 J2.22 XDATA7 B XDATA7 / REV_EN configuration	12	J2.7	P24*	B	P24 / LRDY / DVP_RDY / RXD3 / IM0_CK signals		
14 J.2.9 P.26* B P.26 / LLDS_N / KXD2 / TM1_CK signals 15 J2.10 P27* B P27 / LUDS_N / TXD2 / TM1_CK signals 16 J2.11 XTL32K0 O 32.768KHz crystal output 17 J2.12 XTL32K1 I 32.768KHz crystal input 18 J2.13 VCC18A_RTCI PI 1.8V power output 20 J2.15 LB_CLK B Local bus clock input or output 21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1/LB_MOD configuration 24 J2.19 XDATA2 B XDATA4/BURN_FLASH_21K configuration 25 J2.20 XDATA5 B XDATA5/BURN_FLASH_21K configuration 27 J2.22 XDATA6 B XDATA7/REV_EN configuration 28 J2.23 RST_N I Module reset input 29 J2.24 <	13	J2.8	P25*	B	P25 / LINT / TXD3 / TM0_GT signals		
15 J.10 P2/* B P2//LDDS_N/TXD2/TMLGT signals 16 J2.11 XTL32K0 O 32.768KHz crystal output 17 J2.12 XTL32K1 1 32.768KHz crystal input 18 J2.13 VCC18A_RTCI PI 1.8V power output 0 20 J2.15 LB_CLK B Local bus clock input or output 0 21 J2.16 WED* O WiFi link status LED 0 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA2/SYNC_BUS configuration 24 J2.19 XDATA2 B XDATA2/SYNC_BUS configuration 25 J2.20 XDATA5 B XDATA6/12C_BOOT_DIS configuration 28 J2.23 RST N I Module reset input 29 J2.24 GND G Ground 31 J1.2 P00* B P00/LA8/DE3/TX_CLK/REFCKO signals 32 J1.3 <td>14</td> <td>J2.9</td> <td>P26*</td> <td>B</td> <td colspan="2">P20 / LLDS_N / KXD2 / TM1_CK signals</td>	14	J2.9	P26*	B	P20 / LLDS_N / KXD2 / TM1_CK signals		
16 J.11 XIL32K0 O 32./68KHz crystal ouput 17 J2.12 XTL32KI I 32.768KHz crystal input 18 J2.13 VCCI8A_RTCI PI 1.8V power input for 32.768KHz crystal I/O and RTC logic 19 J2.14 IV8 PO 1.8V power output 20 J2.15 LB_CLK B Local bus clock input or output 21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA2/SYNC_BUS configuration 24 J2.19 XDATA4 B XDATA5/SURN_FLASH_EN configuration 26 J2.21 XDATA5 B XDATA5/BURN_FLASH_EN configuration 27 J2.22 XDATA6 B XDATA7/REV_EN configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 31 J1.2 P00*	15	J2.10	P27*	B	P27 / LUDS_N / TXD2 / TM1_GT signals		
17 J2.12 X1L32K1 1 32./68KHz crystal input 18 J2.13 VCC18A_RTCI PI 1.8V power output for 32./68KHz crystal I/O and RTC logic 19 J2.14 IV8 PO 1.8V power output 20 J2.15 LB_CLK B Local bus clock input or output 21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1/LB_MOD configuration 24 J2.19 XDATA2 B XDATA2/SYNC_BUS configuration 25 J2.20 XDATA5 B XDATA5/BURN_FLASH_921K configuration 26 J2.21 XDATA6 B XDATA6/12C_BOOT_DIS configuration 27 J2.22 XDATA6 B XDATA7/REV_EN configuration 30 J1.1 XDATA7 B XDATA7/REV_EN configuration 31 J1.2 P00* B P00/LA8/DE3/TX_CK/REFCKO signals 32 J1.3 P01* B P01/LA9/RE3_N /MTXD0 signals <t< td=""><td>16</td><td>J2.11</td><td>XTL32KO</td><td>0</td><td>32.768KHz crystal output</td></t<>	16	J2.11	XTL32KO	0	32.768KHz crystal output		
18 J2.13 VCCISA_RICI PI 1.8V power input for 32.768KHz crystal I/O and RIC logic 19 J2.14 IV8 PO 1.8V power output 20 J2.15 LB_CLK B Local bus clock input or output 21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1/LB_MOD configuration 24 J2.19 XDATA2 B XDATA2/SYNC_BUS configuration 25 J2.20 XDATA4 B XDATA5/BURN_FLASH_EN configuration 26 J2.21 XDATA5 B XDATA6/I2C_BOOT_DIS configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B PO1/LA8/DE3/TX_CLK / REFCKO signals 32 J1.3 P01* B P02/LA10 / CTS3 / MTXD1 signals 33 J1.4 <td< td=""><td>17</td><td>J2.12</td><td>XTL32KI</td><td>l</td><td>32.768KHz crystal input</td></td<>	17	J2.12	XTL32KI	l	32.768KHz crystal input		
19J2.14 $1V8$ PO1.8V power output20J2.15 LB_CLK BLocal bus clock input or output21J2.16 $WLED^*$ OWiFi link status LED22J2.17SYSCK_SELIOperating system clock frequency selection input23J2.18XDATA1BXDATA2/SYNC_BUS configuration24J2.19XDATA2BXDATA2/SYNC_BUS configuration25J2.20XDATA4BXDATA5/BURN_FLASH_EN configuration26J2.21XDATA5BXDATA5/BURN_FLASH_921K configuration27J2.22XDATA6BXDATA6/I2C_BOOT_DIS configuration28J2.23RST_NIModule reset input29J2.24GNDGGround30J1.1XDATA7BXDATA7 / REV_EN configuration31J1.2P00*BP00 / LA8 / DE3 / TX_CLK / REFCKO signals32J1.3P01*BP01 / LA9 / RE3_N / MTXD0 signals33J1.4P02*BP02 / LA10 / CTS3 / MTXD1 signals34J1.5P03*BP03 / LA11 / DSR3 / TX_EN signals35J1.6P04*BP06 / LA14 / RTS3 / MRXD0 signals36J1.7P05*BP06 / LA14 / RTS3 / MRXD1 signals38J1.9P07*BP07 / LA15 / DTR3 / RX_DV / CRS_DV signals39J1.10P10*BP10 / LA0 / MCLK / MTXD2 signals40J1.11P11*BP12 / LA2 / WST / TX_ER signals<	18	J2.13	VCC18A_RTCI	PI	1.8V power input for 32.768KHz crystal I/O and RTC logic		
20J2.15LB_CLKBLocal bus clock input or output21J2.16WLED*OWiFi link status LED22J2.17SYSCK_SELIOperating system clock frequency selection input23J2.18XDATA1BXDATA1/LB_MOD configuration24J2.19XDATA2BXDATA1/LB_MOD configuration25J2.20XDATA4BXDATA4/BURN_FLASH_EN configuration26J2.21XDATA5BXDATA5/BURN_FLASH_921K configuration28J2.23RST_NIModule reset input29J2.24GNDGGround30J1.1XDATA7BXDATA7/REV_EN configuration31J1.2P00*BP00/LA8/DE3/TX_CLK/REFCKO signals32J1.3P01*BP01/LA9/RE3_N/MTXD0 signals33J1.4P02*BP04/LA12/R13/RX_CLK/REFCKI signals34J1.5P03*BP04/LA12/R13/MRXD0 signals35J1.6P04*BP06/LA14/RTS3/MRXD1 signals36J1.7P05*BP07/LA15/DTR3/RX_DV/CRS_DV signals38J1.9P07*BP11/LA0/MCLK/MTXD2 signals39J1.10P10*BP10/LA0/MCLK/MTXD3 signals40J1.11P11*BP11/LA1/BCKT/MTXD3 signals41J1.12P12*BP12/LA2/WST/TX_ER signals43J1.16GNDGGround44J1.15SCLBI2C serial clock </td <td>19</td> <td>J2.14</td> <td>1V8</td> <td>PO</td> <td colspan="2">1.8V power output</td>	19	J2.14	1V8	PO	1.8V power output		
21 J2.16 WLED* O WiFi link status LED 22 J2.17 SYSCK_SEL I Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1/LB_MOD configuration 24 J2.19 XDATA2 B XDATA2/SYNC_BUS configuration 25 J2.20 XDATA4 B XDATA5/BURN_FLASH_EN configuration 26 J2.21 XDATA6 B XDATA6/I2C_BOOT_DIS configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7/REV_EN configuration 31 J1.2 P00* B P00/LA8/DE3/TX_CLK/REFCKO signals 32 J1.3 P01* B P01/LA9/RE3_N/MTXD0 signals 33 J1.4 P02* B P02/LA12/R13/RX_EN signals 34 J1.5 P03* B P03/LA11/DSR3/MXD1 signals 35 J1.6 P04* B P0	20	J2.15	LB_CLK	B	Local bus clock input or output		
22 J2.17 SYSCK_SEL 1 Operating system clock frequency selection input 23 J2.18 XDATA1 B XDATA1/LB_MOD configuration 24 J2.19 XDATA2 B XDATA4/BURN_FLASH_EN configuration 25 J2.20 XDATA4 B XDATA4/BURN_FLASH_2N configuration 26 J2.21 XDATA6 B XDATA6/I2C_BOOT_DIS configuration 27 J2.22 XDATA6 B XDATA7/REV_EN configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7/REV_EN configuration 31 J1.2 P00* B P00/LA8/DE3/TX_CLK / REFCKO signals 32 J1.3 P01* B P01/LA9/RE3_N/MTXD0 signals 33 J1.4 P02* B P02/LA10/CTS3/MTXD1 signals 34 J1.5 P03* B P03/LA11/DSR3/TX_EN signals 35 J1.6 P04* B <td>21</td> <td>J2.16</td> <td>WLED*</td> <td>0</td> <td colspan="2">WiFi link status LED</td>	21	J2.16	WLED*	0	WiFi link status LED		
23 J2.18 XDATA1 B XDATA1 / LB_MOD configuration 24 J2.19 XDATA2 B XDATA2 / SYNC_BUS configuration 25 J2.20 XDATA4 B XDATA4 / BURN_FLASH_EN configuration 26 J2.21 XDATA6 B XDATA6 / I2C_BOOT_DIS configuration 27 J2.22 XDATA6 B XDATA6 / I2C_BOOT_DIS configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7 / REV_EN configuration 31 J1.2 P00* B P00 / LA8 / DE3 / TX_CLK / REFCKO signals 32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P06 / LA14 / RTS3 / MRXD1 signals 36 J1.7 P05*	22	J2.17	SYSCK_SEL	I	Operating system clock frequency selection input		
24 J2.19 XDATA2 B XDATA2 / SYNC_BUS configuration 25 J2.20 XDATA4 B XDATA4 / BURN_FLASH_EN configuration 26 J2.21 XDATA5 B XDATA5 / BURN_FLASH_921K configuration 27 J2.22 XDATA6 B XDATA6 / I2C_BOOT_DIS configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7 / REV_EN configuration 31 J1.2 P00* B P00 / LA8 / DE3 / TX_CLK / REFCKO signals 32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P06 / LA14 / RTS3 / MRXD0 signals 36 J1.7 P05* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* </td <td>23</td> <td>J2.18</td> <td>XDATA1</td> <td>В</td> <td colspan="2">XDATA1 / LB_MOD configuration</td>	23	J2.18	XDATA1	В	XDATA1 / LB_MOD configuration		
25 J2.20 XDATA4 B XDATA4 / BURN_FLASH_EN configuration 26 J2.21 XDATA5 B XDATA5/BURN_FLASH_921K configuration 27 J2.22 XDATA6 B XDATA6 / I2C_BOOT_DIS configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7/REV_EN configuration 31 J1.2 P00* B P00 / LA8 / DE3 / TX_CLK / REFCKO signals 32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10	24	J2.19	XDATA2	В	XDATA2 / SYNC_BUS configuration		
26 J2.21 XDATA5 B XDATA5 / BURN_FLASH_921K configuration 27 J2.22 XDATA6 B XDATA6 / I2C_BOOT_DIS configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7/REV_EN configuration 31 J1.2 P00* B P00 / LA8 / DE3 / TX_CLK / REFCKO signals 32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD3 signals 40 J1.11	25	J2.20	XDATA4	В	XDATA4 / BURN_FLASH_EN configuration		
27 J2.22 XDATA6 B XDATA6/I2C_BOOT_DIS configuration 28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7/REV_EN configuration 31 J1.2 P00* B P00/LA8/DE3/TX_CLK/REFCKO signals 32 J1.3 P01* B P01/LA9/RE3_N/MTXD0 signals 33 J1.4 P02* B P02/LA10/CTS3/MTXD1 signals 34 J1.5 P03* B P03/LA11/DSR3/TX_EN signals 35 J1.6 P04* B P04/LA12/RI3/RX_CLK/REFCKI signals 36 J1.7 P05* B P05/LA13/DCD3/MRXD0 signals 37 J1.8 P06* B P06/LA14/RTS3/MRXD1 signals 38 J1.9 P07* B P07/LA15/DTR3/RX_DV/CRS_DV signals 39 J1.10 P10* B P10/LA0/MCLK/MTXD3 signals 41 J1.12 P12* B P12/LA2/WST/TX_ER signals	26	J2.21	XDATA5	В	XDATA5 / BURN_FLASH_921K configuration		
28 J2.23 RST_N I Module reset input 29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7 / REV_EN configuration 31 J1.2 P00* B P00 / LA8 / DE3 / TX_CLK / REFCKO signals 32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* <td>27</td> <td>J2.22</td> <td>XDATA6</td> <td>В</td> <td>XDATA6 / I2C_BOOT_DIS configuration</td>	27	J2.22	XDATA6	В	XDATA6 / I2C_BOOT_DIS configuration		
29 J2.24 GND G Ground 30 J1.1 XDATA7 B XDATA7 / REV_EN configuration 31 J1.2 P00* B P00 / LA8 / DE3 / TX_CLK / REFCKO signals 32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13	28	J2.23	RST_N	Ι	Module reset input		
30 J1.1 XDATA7 B XDATA7 / REV_EN configuration 31 J1.2 P00* B P00 / LA8 / DE3 / TX_CLK / REFCKO signals 32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD3 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43	29	J2.24	GND	G	Ground		
31 J1.2 P00* B P00/LA8/DE3/TX_CLK/REFCKO signals 32 J1.3 P01* B P01/LA9/RE3_N/MTXD0 signals 33 J1.4 P02* B P02/LA10/CTS3/MTXD1 signals 34 J1.5 P03* B P03/LA11/DSR3/TX_EN signals 35 J1.6 P04* B P04/LA12/RI3/RX_CLK/REFCKI signals 36 J1.7 P05* B P05/LA13/DCD3/MRXD0 signals 37 J1.8 P06* B P06/LA14/RTS3/MRXD1 signals 38 J1.9 P07* B P07/LA15/DTR3/RX_DV/CRS_DV signals 39 J1.10 P10* B P10/LA0/MCLK/MTXD2 signals 40 J1.11 P11* B P11/LA1/BCKT/MTXD3 signals 41 J1.12 P12* B P12/LA2/WST/TX_ER signals 42 J1.13 P13* B P13/LA3/DATAT/COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data	30	J1.1	XDATA7	В	XDATA7 / REV_EN configuration		
32 J1.3 P01* B P01 / LA9 / RE3_N / MTXD0 signals 33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND	31	J1.2	P00*	В	P00 / LA8 / DE3 / TX_CLK / REFCKO signals		
33 J1.4 P02* B P02 / LA10 / CTS3 / MTXD1 signals 34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD3 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI	32	J1.3	P01*	В	P01 / LA9 / RE3_N / MTXD0 signals		
34 J1.5 P03* B P03 / LA11 / DSR3 / TX_EN signals 35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P13 / LA3 / DATAT / COL signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power i	33	J1.4	P02*	В	P02 / LA10 / CTS3 / MTXD1 signals		
35 J1.6 P04* B P04 / LA12 / RI3 / RX_CLK / REFCKI signals 36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	34	J1.5	P03*	В	P03 / LA11 / DSR3 / TX_EN signals		
36 J1.7 P05* B P05 / LA13 / DCD3 / MRXD0 signals 37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	35	J1.6	P04*	В	P04 / LA12 / RI3 / RX_CLK / REFCKI signals		
37 J1.8 P06* B P06 / LA14 / RTS3 / MRXD1 signals 38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	36	J1.7	P05*	В	P05 / LA13 / DCD3 / MRXD0 signals		
38 J1.9 P07* B P07 / LA15 / DTR3 / RX_DV / CRS_DV signals 39 J1.10 P10* B P10 / LA0 / MCLK / MTXD2 signals 40 J1.11 P11* B P11 / LA1 / BCKT / MTXD3 signals 41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	37	J1.8	P06*	В	P06 / LA14 / RTS3 / MRXD1 signals		
39 J1.10 P10* B P10/LA0/MCLK/MTXD2 signals 40 J1.11 P11* B P11/LA1/BCKT/MTXD3 signals 41 J1.12 P12* B P12/LA2/WST/TX_ER signals 42 J1.13 P13* B P13/LA3/DATAT/COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	38	J1.9	P07*	В	P07 / LA15 / DTR3 / RX_DV / CRS_DV signals		
40 J1.11 P11* B P11/LA1/BCKT/MTXD3 signals 41 J1.12 P12* B P12/LA2/WST/TX_ER signals 42 J1.13 P13* B P13/LA3/DATAT/COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	39	J1.10	P10*	В	P10 / LA0 / MCLK / MTXD2 signals		
41 J1.12 P12* B P12 / LA2 / WST / TX_ER signals 42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	40	J1.11	P11*	В	P11 / LA1 / BCKT / MTXD3 signals		
42 J1.13 P13* B P13 / LA3 / DATAT / COL signals 43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	41	J1.12	P12*	В	P12 / LA2 / WST / TX_ER signals		
43 J1.14 SDA B I2C serial clock 44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	42	J1.13	P13*	В	P13 / LA3 / DATAT / COL signals		
44 J1.15 SCL B I2C serial data 45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	43	J1.14	SDA	В	I2C serial clock		
45 J1.16 GND G Ground 46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	44	J1.15	SCL	В	I2C serial data		
46 J1.17 3V3 PI 3.3V power input 47 J1.18 3V3 PI 3.3V power input	45	J1.16	GND	G	Ground		
47 J1.18 3V3 PI 3.3V power input	46	J1.17	3V3	PI	3.3V power input		
	47	J1.18	3V3	PI	3.3V power input		
48 J1.19 GND G Ground	48	J1.19	GND	G	Ground		



AXM22001-2A-C IEEE 802.11b/g WiFi Module Board User's Guide

40	11.20	CND	C	Gaunal	
49	J1.20	GND	G		
50	J4.1	PI4*	B	P14 / LA4 / BCKR / MRXD2 signals	
51	J4.2	P15*	В	P15 / LRD_N / WSR / MRXD3 signals	
52	J4.3	P16*	В	P16 / LWR_N / DATAR / RX_ER signals	
53	J4.4	P17*	В	P17 / LCS0_N / HREF / CRS signals	
54	J4.5	RXD0	В	MCPU UART 0 serial receive data	
55	J4.6	TXD0	0	MCPU UART 0 serial transmit data	
56	J4.7	INT0*	В	INT0 / XWKUP / LDA8 / SINT / DB_DI signals	
57	J4.8	INT1*	В	INT1 / WINT0 / LDA9 / SRDY / DB_CKO signals	
58	J4.9	SS1*	В	SS1 / LDA10 / STPZ / DB_DO signals	
59	J4.10	SS2*	В	SS2 / LDA11 / DQ / MINT_N signals	
60	J4.11	SS0*	В	SS0 / LDA12 signals	
61	J4.12	RSTO_N	0	Reset output	
62	J4.13	SCLK*	В	SCLK / LDA13 / WDB_DI signals	
63	J4.14	MOSI*	В	MOSI / LDA14 / WDB_CKO signals	
64	J4.15	MISO*	В	MISO / LDA15 / WDB_DO signals	
65	J4.16	P37*	В	P37 / LDA7 / Y7 / DTR2 / CEX4 signals	
66	J4.17	P36*	В	P36 / LDA6 / Y6 / RTS2 / CEX3 signals	
67	J4.18	P35*	В	P35 / LDA5 / Y5 / DCD2 / CEX2 signals	
68	J4.19	P34*	В	P34 / LDA4 / Y4 / RI2 / CEX1 signals	
69	J4.20	P33*	В	P33 / LDA3 / Y3 / DSR2 / CEX0 signals	
70	J4.21	P32*	В	P32 / LDA2 / Y2 / CTS2 / ECI signals	
71	J4.22	P31*	В	P31 / LDA1 / Y1 / RE2 N / TM2 GT signals	
72	J4.23	P30*	В	P30 / LDA0 / Y0 / DE2 / TM2 CK signals	
73	J4.24	3V3 RF	PI	3.3V power input for RF circuit	
74	J4.25	3V3_RF	PI	3.3V power input for RF circuit	
75	J4.26	GND	G	Ground	
76	J4.27	GND	G	Ground	
77	J4.28	GND	G	Ground	
78	J4.29	GND	G	Ground	

Note:

* These pins are multi-function pins in AX22001. Please refer to Section 3.1.3 "Multi-function Pin Setting $(0x07 \sim 0x02)$ " on AX22001 datasheet to configure proper pin functions for your AX22001 application.

Please feel free to contact ASIX Electronics Technical Support (<u>support@asix.com.tw</u>) to receive AXM22001-2A-C WiFi module board schematic and BOM file for details.



Board Dimensions

The AXM22001-2A-C is a surface mountable module with castellated mounting holes on three sides. Below shows the module dimensions.



51.04mm



Figure 2. Module Dimension



Host PCB Footprint

Below shows the recommended host PCB footprints for the module. The AXM22001-2A-C module has an integrated PCB antenna which requires the host PCB to maintain certain copper keep-out area as shown below, for best antenna performance. Also, when mounting on the host PCB of user's system, the module's PCB antenna should be on the edge of the host PCB and faced outward.



Figure 3. Layout Footprint & layout guide



Module Reflow Profile



Zone	#AD1	#AD2	#AD3	#AD4	#AD5	#AD6	#AD7	#AD8
Upper Limit(°C)	170	175	185	190	195	225	275	260
Lower Limit(°C)	170	0	0	0	0	225	275	260
Time (S)	50	50	50	50	50	50	50	50

rigure 4. Module Kellow	Figure	4.	Module	Reflow
-------------------------	--------	----	--------	--------



PCB Antenna

One of the main reasons to use a PCB antenna is to reduce cost. Since the antennas is fabricated on the top layer with solder mask. Other layers below the antenna have no copper trace and plane. It is recommended that the module be mounted on the edge of the host PCB. To have best performance, place the module on the host PCB according to the details shown in Figure 3. The antenna patterns are shown in the Figure 5 and Figure 6. These patterns allow the designer to understand the performance of the module with respect to the position of the receive/transmit antenna at the other end of the link.



Figure 5. Module in horizontal antenna pattern



Figure 6. Module in vertical antenna pattern



Regulatory Approval

The AXM22001-2A-C module has acquired the regulatory approvals for modular devices in the United States. Modular approval allows the user to mount the AXM22001-2A-C module inside his own final product and needn't the regulatory testing, if no changes or modifications to the module circuitry. Any changes or modifications will cause the user to lose his authority to operate the equipment. The user must comply with all of the instructions provided by ASIX Electronics, which indicate the necessary of the installation and/or operating conditions for the compliance.

The integrator still has the responsibility to test the end product for any additional compliance (for example: digital device emission, PC peripheral requirements, etc.) in the specific country that the end product will be sold.

United States

The AXM22001-2A-C module has complied with part 15 subpart C "Intentional Radiators" 15.247, 15.207 and 15.209 of the FCC Rules. And modular approval with FCC part 15.212. The module can be integrated into a finished product without obtaining subsequent and separate FCC approvals. For product available in the USA market, only channel 1~11 can be operated. Selection of other channels is not possible.

FCC Statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- •Reorient or relocate the receiving antenna.
- •Increase the separation between the equipment and receiver.
- •Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- •Consult the dealer or an experienced radio/TV technician for help

The user's manual or datasheet of the end product should include the above statement.

FCC Caution

To ensure continued compliance, (1) Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. (2)This device must not be co-located or operating in conjunction with any other antenna or transmitter.

Co-location with other radio transmitting devices operating concurrently in the same band will require additional testing and certification.

FCC Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- 1. This device may not cause harmful interference.
- 2. This device must accept any interference received, including interference that may cause undesired operation.



FCC Label requirement:

If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: Z59A22001C" or "Contains FCC ID: Z59A22001C." Any similar wording that expresses the same meaning may be used.

Contains Transmitter Module FCC ID: Z59A22001C or Contains FCC ID: Z59A22001C

RF Exposure:

The following statement must be included as a CAUTION statement in manuals and OEM products to alert users of FCC RF exposure compliance:

To satisfy FCC RF Exposure requirements for mobile and base station transmission devices, the distance between the antenna of for this device and the persons must be 20 cm or more during operation.

This device must not be co-located or operating in conjunction with any other antenna or transmitter.

If the AXM22001-2A-C module is used in a portable application (i.e., the antenna is less than 20 cm from persons during operation), the integrator is responsible for performing Specific Absorption Rate (SAR) testing in accordance with FCC rules 2.1091.

Helpful Web Sites:

Federal Communications Commission (FCC): http://www.fcc.gov

Europe

The AXM22001-2A-C module has been certified for using in European countries. The following testing has been completed:

Test standard ETSI EN 300 328 V1.7.1 (2006):

- •Equivalent Isotropic Radiated Power
- •Maximum Spectral Power Density
- •Frequency Range
- •Transmitter Spurious Emissions
- •Receiver Spurious Emissions

Test standards ETSI EN 301 489-1:2008 and ETSI EN 301 489-17:2009:

- •Radiated Emissions
- •Electrostatic Discharge (ESD)
- •RF Electromagnetic Field (RS)

The modules are fully compliant with

- •Radiated Emissions EN 55022
- •Electrostatic Discharge EN 61000-4-2

•RF Electromagnetic Field EN 61000-4-3



ETSI does not provide a modular approval service. However, the testing completed above included the test plan, test results and can be the reference for the certification. The end user is responsible for ensuring compliance with harmonized frequencies and labeling requirements for each country in which the end device is marketed and sold.

Helpful Web Sites:

Radio and Telecommunications Terminal Equipment (R&TTE):http://ec.europa.eu/enterprise/rtte/index_en.htm European Conference of Postal and Telecommunications Administrations (CEPT):http://www.cept.org/ European Telecommunications Standards Institute (ETSI): http://www.etsi.org/ European Radio Communications Office (ERO): <u>http://www.ero.dk/</u>